U.S. Express Mail No.: EI215536970US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application Of

Inventors: Peijun Ding
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Serial No.: Not Yet Assigned

Filed: Herewith

Title: A TAILORED BARRIER LAYER WHICH PROVIDES IMPROVED COPPER INTERCONNECT ELECTROMIGRATION RESISTANCE

PATENT APPLICATION

Docket No. AM-1776

CERTIFICATE OF MAILING BY "EXPRESS MAIL" UNDER 37 C.F.R. § 1.10

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APPLICATION TRANSMITTAL LETTER

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Transmitted herewith for filing is the patent application identified as follows:

Inventor(s): Peijun Ding
Tony Chiang
Barry L. Chin

Title: A TAILORED BARRIER LAYER WHICH PROVIDES IMPROVED COPPER INTERCONNECT ELECTROMIGRATION RESISTANCE

No. of pages of Specification: 16 ; No. of pages of Claims: 6 ; No. of pages of Abstract: 1.

U.S. Express Mail No.: EI215536970US

No. of Sheets of Drawings: 2 ; Formal: __, Informal: X .

Also enclosed are:

_X_ A Declaration and Power of Attorney.

_X_ An Assignment. Recording of the Assignment is hereby requested.

____ A Power of Attorney.

____ An Information Disclosure Statement under 37 C.F.R. §1.56.

FEES DUE

The fees due for filing the specification pursuant to 37 C.F.R. §1.16 and for recording of the Assignment, if any, are determined as follows:

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	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEES
Basic Application Fee					$ 790.00
Total Claims	31	MINUS 20=	11	x $22 =	242.00
Independent Claims	5	MINUS 3 =	2	x $82 =	164.00
If multiple dependent claims are presented, add $270.00					270.00
Add Assignment Recording Fee of $40.00 if Assignment document is enclosed					40.00
TOTAL APPLICATION FEE DUE					1,506.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is $1,506.00, and is provided as follows:

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U.S. Express Mail No.: EI215536970US

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Date: Dec 19, 1997

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Express Mail No. EI215536970US

United States Patent Application for:

A TAILORED BARRIER LAYER WHICH PROVIDES IMPROVED COPPER INTERCONNECT ELECTROMIGRATION RESISTANCE

Inventors: Peijun Ding

Tony Chiang

Barry L. Chin

Attorney Docket No. AM-1776

Certification Under 37 CFR 1.10

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A TAILORED BARRIER LAYER WHICH PROVIDES IMPROVED COPPER INTERCONNECT ELECTROMIGRATION RESISTANCE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains to a particular TaN_x/Ta barrier/wetting layer structure which increases the degree of {111} crystal orientation in an overlying copper layer, thereby providing improved electromigration resistance of the copper.

2. Brief Description of the Background Art

As microelectronics continue to miniaturize, interconnection performance, reliability, and power consumption has become increasingly important, and interest has grown in replacing aluminum alloys with lower-resistivity and higher-reliability metals. Copper offers a significant improvement over aluminum as a contact and interconnect material. For example, the resistivity of copper is about 1.67 $\mu\Omega$cm, which is only about half of the resistivity of aluminum.

There are two principal competing technologies under evaluation by material and process developers working to enable the use of copper. The first technology is known as damascene technology. In this technology, a typical process for producing a multilevel structure having feature sizes (*i.e.*, width of the aperture) in the range of 0.5 micron (μm) or less would include: blanket deposition of a dielectric material; patterning of the dielectric material to form openings; deposition of a diffusion barrier layer and, optionally, a wetting layer to line the openings; deposition of a copper layer onto the substrate in sufficient thickness to fill the openings; and removal of excessive conductive material from the substrate surface using chemical-mechanical polishing

(CMP) techniques. The damascene process is described in detail by C. Steinbruchel in "Patterning of copper for multilevel metallization: reactive ion etching and chemical-mechanical polishing", *Applied Surface Science* 91 (1995) 139 - 146.

The competing technology is one which involves the patterned etch of a copper layer. In this technology, a typical process would include deposition of a copper layer on a desired substrate (typically a dielectric material having a barrier layer on its surface); application of a patterned hard mask or photoresist over the copper layer; pattern etching of the copper layer using wet or dry etch techniques; and deposition of a dielectric material over the surface of the patterned copper layer, to provide isolation of conductive lines and contacts which comprise various integrated circuits.

Typically, the copper layer can be applied using sputtering techniques well known in the art. The sputtering of copper provides a much higher deposition rate than evaporation or CVD (chemical vapor deposition) and provides a purer copper film than CVD.

In integrated circuit interconnect structures where copper is the material used to form conductive lines and contacts, it is recognized that copper diffuses rapidly into adjacent layers of SiO_2 and silicon and needs to be encapsulated. Gang Bai et al. in "Copper Interconnection Deposition Techniques and Integration", 1996 Symposium on VLSI Technology, Digests of Technical Papers (0-7803-3342-X/96, IEEE), describe the effectiveness of Ta, TiN, W and Mo as barrier layers for use with copper. They concluded that Ta annealed in UHV (ultra high vacuum) after copper deposition provided the best barrier layer. Sputtered copper appeared to be preferable over CVD copper and over electroplated copper, although all the data for electroplated copper was not available at the time of presentation of the paper.

U.S. Patent No. 4,319,264 of Gangulee et al., issued March 9, 1982 and titled "Nickel-gold-nickel Conductors For Solid State Devices" discusses the problem of electromigration in solid state devices. In particular, the patent discusses the application of direct current over particular current density ranges which induces motion of the atoms comprising the thin film conductor, the effect known as electromigration. Electromigration is said to induce crack or void formation in the conductor which, over a period of time, can result in conductor failure. The rate of electromigration is said to be dependent on the current density imposed on the conductor, the conductor temperature, and the properties of the conductor material. In high current density applications, potential conductor failure due to electromigration is said to severely limit the reliability of the circuit. In discussing the various factors affecting performance of the conductive materials, grain structure is mentioned as being important. (In order to obtain adequate lithographic line width resolution, it is recommended that the film be small grained, with a grain size not exceeding about one-third of the required line width.) Uniformity of grain size and preferred crystallographic orientation of the grains are also said to be factors which promote longer (electromigration limited) conductor lifetimes. Fine grained films are also described as being smoother, which is a desirable quality in semiconductor applications, to lessen difficulties associated with covering the conductor with an overlayer.

U.S. Patent No. 5,571,752 to Chen et al., issued November 5, 1996, discloses a method for patterning a submicron semiconductor layer of an integrated circuit. In one embodiment describing an aluminum contact, titanium or titanium nitride having a thickness of between approximately 300 and 2,000 Å is formed by sputter deposition to reach the bottom of a contact opening. Finally, a second conductive layer, typically aluminum, is applied over the surface of the conformal conductive layer. The aluminum

is sputtered on, preferably at a temperature ranging between approximately 100°C and 400°C. This method is said to make possible the filling of contact openings having smaller device geometry design requirements by avoiding the formation of fairly large grain sizes in the aluminum film.

As described in U.S. Patent Application Serial No. 08/824,911, of Ngan et al., filed March 27, 1997 and commonly assigned with the present invention, efforts have been made to increase the {111} crystallographic content of aluminum as a means of improving electromigration of aluminum. In particular, the {111} content of an aluminum layer was controlled by controlling the thickness of various barrier layers underlying the aluminum layer. The underlying barrier layer structure was $Ti/TiN/TiN_x$, which enabled aluminum filling of high aspect vias while providing an aluminum fill exhibiting the high degree of aluminum {111} crystal orientation. The $Ti/TiN/TiN_x$ barrier layer was deposited using IMP (ion metal plasma) techniques, and the barrier layer thicknesses were as follows. The thickness of the first layer of Ti ranges from greater than about 100 Å to about 500 Å (the feature geometry controls the upper thickness limit). The thickness of the TiN second layer ranges from greater than about 100 Å to less than about 800 Å (preferably, less than about 600 Å). And, the TiN_x third layer (having a Ti content ranging from about 50 atomic percent titanium to about 100 atomic percent titanium) ranges from about 15 Å to about 500 Å. A $Ti/TiN/TiN_x$ barrier layer having this structure, used to line a contact via, is described as enabling complete filling of via with sputtered warm aluminum, where the feature size of the via or aperture is about 0.25 micron or less and the aspect ratio ranges from about 5 : 1 to as high as about 6 : 1.

Subsequently, in U.S. Patent Application Serial No. 08/924,487, of Ngan et al., filed August 23, 1997 (Docket No. 1987), the inventors disclose that to maintain a

consistently high aluminum {111} crystal orientation content of an interconnect during the processing of a series of semiconductor substrates in a given process chamber, it is necessary to form the first deposited layer of the barrier layer to a minimal thickness of at least about 150 Å, to compensate for irregularities in the crystal orientation which may be present during the initial deposition of this layer when the process chamber is initially started up (and continuing for the first 7 - 8 wafers processed). Ngan et al. teach that in the case of a copper conductive layer, it may also be necessary that the first layer of a barrier layer structure underlying the copper layer have a minimal thickness of at least about 150 Å, to enable a consistent crystal orientation within the copper layer during the processing of a series of wafers in a semiconductor chamber.

SUMMARY OF THE INVENTION

We have discovered that tantalum nitride (TaN_x) is a better barrier layer for copper than tantalum (Ta). However, copper deposited directly over TaN_x does not exhibit a sufficiently high degree of {111} crystal orientation to provide the desired copper electromigration characteristics. We have developed a barrier layer structure comprising a layer of Ta overlying a layer of TaN_x which provides both a barrier to the diffusion of a copper layer deposited thereover, and enables the formation of a copper layer having a high {111} crystallographic content, so that copper electromigration resistance is increased.

The TaN_x layer, where x ranges from about 0.1 to about 1.5, is sufficiently amorphous to prevent the diffusion of copper into underlying silicon or silicon oxide surfaces. The desired thickness for the TaN_x layer is dependent on the device structure. For a typical interconnect, the TaN_x layer thickness ranges from about 50 Å to about 1,000 Å. For a contact, the TaN_x layer, the thickness on the wall of a contact via ranges

from about 10 Å to about 300 Å, depending on the feature size. The TaN_x layer is preferably deposited using standard reactive ion sputtering techniques at a substrate temperature ranging from about 20°C to about 500°C. However, ion deposition sputtering techniques may be used to deposit this layer.

The Ta layer deposited over the TaN_x layer has a desired thickness ranging from about 5 Å to about 500Å, wherein the thickness is preferably greater than about 20 Å, depending on the feature size. The Ta layer is preferably deposited using standard ion sputtering techniques at a substrate temperature ranging from about 20°C to about 500°C. However, ion deposition sputtering techniques may be used to deposit this layer.

The copper layer is deposited at the thickness desired to suit the needs of the device. The copper layer may be deposited using any of the preferred techniques known in the art. Preferably, the entire copper layer or at least a "seed" layer of copper is deposited using physical vapor deposition techniques such as sputtering or evaporation, as opposed to CVD. Since the crystal orientation of the copper is sensitive to deposition temperature, it is important that the maximum temperature of the copper either during deposition or during subsequent annealing processes not be higher than about 500°C. Preferably, the maximum temperature is about 300°C.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a schematic of a cross sectional view of a sputtering chamber of the kind which can be used to deposit the barrier layer of the present invention.

Figure 2 shows a graph representative of the copper {111} crystal orientation on a TaN_x /Ta barrier layer as a function of the thickness of the Ta layer, with the TaN_x layer held constant at about 500 Å.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present disclosure pertains to a TaN_x/Ta/Cu structure and a method of creating that structure. The TaN_x/Ta barrier layer structure enables the deposition of an overlying copper layer having a high {111} crystallographic content, so that electromigration resistance of the copper is increased.

I. DEFINITIONS

As a preface to the detailed description, it should be noted that, as used in this specification and the appended claims, the singular forms "a", "an", and "the" include plural referents, unless the context clearly dictates otherwise. Thus, for example, the term "a semiconductor" includes a variety of different materials which are known to have the behavioral characteristics of a semiconductor, reference to a "plasma" includes a gas or gas reactants activated by an RF glow discharge, reference to "the contact material" or "interconnect material" includes copper and copper alloys, and other conductive materials which have a melting point enabling them to be sputtered over the temperature range described herein.

Specific terminology of particular importance to the description of the present invention is defined below.

The term "aspect ratio" refers to the ratio of the height dimension to the width dimension of particular openings into which an electrical contact is to be placed. For example, a via opening which typically extends in a tubular form through multiple layers has a height and a diameter, and the aspect ratio would be the height of the tubular divided by the diameter. The aspect ratio of a trench would be the height of the trench divided by the minimal travel width of the trench at its base.

The term "contact via" or "via" refers to an electrical contact having an aspect ratio which is typically greater than 1:1. A contact via most frequently extends through multiple layers of material to connect one electrically conductive element with another.

The term "copper" includes alloys of copper of the kind typically used in the semiconductor industry. The preferred embodiments described herein were for a copper alloy comprising about 98% by weight copper.

The term "feature" refers to contacts, vias, trenches, and other structures which make up the topography of the substrate surface.

The term "interconnect" generally refers to conductive structures within a semiconductive device. For purposes of this patent application, electrical contacts in the form of a "contact via" or "via" (which has a higher aspect ratio than conductive lines in trenches, for example) is distinguished from other conductive structures which form interconnects.

The term "ion-deposition sputtered" and the term "reactive ion metal plasma (IMP)" refer to sputter deposition using a particular technique, wherein a high density, inductively coupled RF plasma is positioned between the sputtering cathode and the substrate support electrode, whereby at least a portion of the sputtered emission is in the form of ions at the time it reaches the substrate surface. Typically, 10% or more of the sputtered emission is in the form of ions at the time it reaches the substrate surface.

The term "traditional sputtering" refers to a method of forming a film layer on a substrate wherein a target is sputtered and the material sputtered from the target passes between the target and the substrate to form a film layer on the substrate, and no means is provided to ionize a substantial portion of the target material sputtered from the target before it reaches the substrate. One apparatus configured to provide traditional sputtering is disclosed in U.S. Patent No. 5,320,728, the disclosure of which is

incorporated herein by reference. In such a traditional sputtering configuration, the percentage of target material which is ionized is less than 10%, more typically less than 1%, of that sputtered from the target.

The term "XRD" (X-ray Diffraction) refers to a technique commonly used to measure crystalline orientation, wherein radiation over particular wavelengths is passed through the material to be characterized, and the diffraction of the radiation, caused by the material through which it passes, is measured. A map is created which shows the diffraction pattern, and the crystal orientation is calculated based on this map.

A "traditionally sputtered" tantalum nitride-comprising film or layer is deposited on a substrate by contacting a tantalum target with a plasma created from an inert gas such as argon in combination with nitrogen gas. A portion of the tantalum sputtered from the target reacts with nitrogen gas which has been activated by the plasma to produce tantalum nitride, and the gas phase mixture contacts the substrate to form a layer on the substrate.

II. AN APPARATUS FOR PRACTICING THE INVENTION

A process system in which the method of the present invention may be carried out is the Applied Materials, Inc. (Santa Clara, California) Endura® Integrated Processing System. This process system is not specifically shown in the Figures. However, the system is generally known in the semiconductor processing industry and is shown and described in United States Patents Nos. 5,186,718 and 5,236,868, the disclosures of which are incorporated by reference. A schematic of a typical sputtering apparatus useful in forming the smooth-surfaced TaN_x/Ta barrier layer of the present invention is shown in Figure 1. Sputtering apparatus 100 includes a sputtering target 110 which has two major surfaces, a back surface 112 from which heat is removed, and a

front surface 114 which is the sputtering surface. The sputtered material is deposited on the surface of semiconductor workpiece 116 which is supported on platen 118. The spacing between the workpiece 116 and the target 110 may be adjusted by moving the platen 118. The sputtering target (cathode) 110 operates at power levels up to about 24 kW. An ionized gas, typically generated from an inert gas such as argon is used to impact sputtering target 110, to produce sputtered metal atoms which are deposited on workpiece 116. The inert gas enters vacuum chamber 117 in the vicinity to target 112 through openings which are not shown on Figure 1. Additional gas may enter vacuum chamber 117 from the surface of workpiece support platen 118, which includes openings (not shown) in its surface to permit the flow of heat transfer gas between workpiece 116 and support platen 118. Such gases are evacuated through an opening (not shown) in vacuum chamber 117, which opening is connected to a conduit (not shown) leading to a vacuum pump (not shown). Vacuum chamber 117 can be operated at pressures ranging from about 0.1 mT to about 60 mT, depending on the particular process involved.

III. A METHOD FOR PRACTICING THE INVENTION

EXAMPLE ONE: FORMATION OF A TaN_x/Ta BARRIER LAYER

To form the TaN_x/Ta barrier layer structure, a tantalum target cathode 110 was used, and a DC power was applied to this cathode over a range from about 0.5 kW to about 8 kW. The spacing between target cathode 110 and workpiece 116 was approximately 200 - 300 mm. During the formation of the TaN_x first layer, argon gas feed to vacuum chamber 117 was about 15 sccm to the substrate support platen 118 and about 7 sccm to the openings in the vicinity of target cathode 110. Nitrogen gas was also fed into vacuum chamber 117 in the vicinity of target cathode 110. The nitrogen gas feed rate ranged from about 2 to about 20 sccm, depending on the DC power applied,

with the nitrogen feed rate being increased as the DC power was increased. With the DC power set at 4 kW and a nitrogen feed rate of about 14 sccm, the TaN_x layer produced was $TaN_{0.7}$, containing about 40 atomic percent nitrogen.

The substrate 116 was a 200 mm diameter silicon wafer having a silicon dioxide dielectric layer on its surface. The substrate was placed a distance of about 10 inches (25 cm) from target cathode 110. The operational pressure in vacuum chamber 117 was about 1.7 mT, and the substrate temperature of the silicon wafer was about 25 °C. Under these conditions, a 500 Å thick layer of TaN was applied in approximately one minute.

Subsequent to application of the TaN layer, the nitrogen gas was shut off, the power to tantalum target cathode 110 was reduced from about 4 kW to about 1 kW, and the argon gas feed was maintained. The pressure in the vacuum chamber remained at about 1.7 mT, and the substrate temperature remained at about 25 °C. Under these conditions, a 60 Å thick layer of tantalum was formed over the TaN layer in about 10 seconds.

The data generated in Figure 2 was for TaN/Ta barrier layers produced in the manner described above, where the length of time for tantalum deposition was increased to produce a thicker tantalum layer, as appropriate.

EXAMPLE TWO: FORMATION OF THE COPPER CONDUCTIVE LAYER

The copper layer overlying the TaN barrier layer was applied using the same apparatus described with regard to application of the TaN barrier layer. The target cathode 110 was copper. During the formation of the overlying Cu layer, argon gas feed to vacuum chamber 117 was about 15 sccm to the substrate support platen 118 and about 90 sccm to the openings in the vicinity of target cathode 110. The substrate, having a tantalum layer as its upper surface, was placed a distance of about 10 inches (25 cm)

from target cathode 110. The operational pressure in vacuum chamber 117 was about 1.0 mT, and the substrate temperature was about 150°C. Under these conditions, a 1,000 Å thick layer of copper was applied in about one minute.

With reference to the formation of the TaN_x/Ta/Cu structure in general, it is advisable to use the minimal thickness possible for the tantalum layer, as a flatter structure is preferred for planarization and imaging purposes, and it is difficult to remove excess tantalum from the surface of the workpiece. When chemical mechanical polishing is used to remove material on the surface of the workpiece between features (known as the "field"), the removal rate for tantalum is much slower than the copper removal rate. As a result, in order to ensure complete removal of copper and Ta/TaN_x from the field, the copper may be over polished, creating a "dishing effect" in the area of a contact, where the copper is removed from the contact to a level below the surface of the substrate/workpiece. In addition, there is a cost in substrate processing time.

The minimal thickness for the tantalum layer is determined by the desired performance features for the layer. The layer must be sufficiently thick to provide a tantalum {002} crystalline orientation which enables easy wetting of the tantalum surface by the copper and depositing of a copper layer having a high {111} crystal orientation. Although a higher temperature is required to dewet/delaminate a depositing copper layer from a Ta surface than from a TaN_x surface, copper delamination is a problem in some instances. Typically, the copper layer is deposited at temperatures in the range of about 300°C to about 500°C (or a copper seed layer is deposited at lower temperatures, but additional copper is deposited and the combination is annealed at temperatures in this range), where delamination of the copper layer is a real possibility. When the copper is deposited for flat interconnect lines, the wetting criteria is not as important as it is when the copper is deposited to fill a contact via having a high aspect

ratio (*i.e.*, depth greater than width).

As the thickness of the tantalum layer increases, the wetting of the tantalum by a layer of copper applied thereover generally improves. As the thickness of the tantalum layer increases, the copper {111} crystallographic content generally increases as well. The limitation on tantalum layer thickness is defined by the device feature size, in particular. If the TaN_x or the Ta layer is too thick, the overall resistance of the conductive feature increases. If these layers are too thin, the barrier may not be adequate to prevent diffusion; further, if the Ta layer is too thin, the copper {111} crystallographic content may be inadequate to provide the desired electromigration resistance.

In general, the copper {111} crystallographic content is poorer when copper is applied directly over a TaN_x layer due to the amorphous structural content of the TaN_x layer. Further, copper applied by means other than sputtering, where the copper layer itself has a higher impurity level (such as copper applied by CVD), may result in an unacceptably low copper {111} crystallographic content. The use of a Ta layer over the TaN_x layer can produce an acceptable surface for growth of a high copper {111} crystallographic content. Deposition of a seed layer of copper over the Ta surface prior to application of the entire copper contact by other means, such as CVD, provides a starting matrix for copper growth, since some CVD precursors and electroplating require a conductive substrate for the copper deposition process to take place. Further, the copper seed layer promotes an increase in the copper {111} crystallographic content.

IV. THE STRUCTURE OF THE TaN_x)/Ta BARRIER LAYER AND ITS EFFECT ON THE COPPER {111} CRYSTALLOGRAPHIC CONTENT

Figure 2 shows a graph 200 of the {111} crystallographic content (measured by XRD) of a copper layer as a function of the thickness of the Ta layer of a TaN_x/Ta barrier layer.

In particular, the various specimens examined (prepared using the method described above) are represented on the scale labeled 207. The layers of material were deposited using standard, traditional sputtering techniques. In all instances, the copper layer was 1,000 Å thick. In all instances, except the data point labeled 206, the underlying layer of TaN_x was 500 Å thick. The data point labeled 206 represents a 500 Å thick Ta (only) barrier layer. The data point labeled 208 represents a 500 Å thick TaN_x (only) barrier layer. The data point labeled 210 represents the TaN_x/TaN structure where the overlying Ta layer was 57 Å thick. The data point labeled 212 represents the TaN_x/Ta structure where the overlying Ta layer was 114 Å thick. The data point labeled 214 represents the TaN_x/Ta structure where the overlying Ta layer was 170 Å thick. The data point labeled 216 represents the TaN_x/Ta structure where the overlying Ta layer was 227 Å thick. And, the data point labeled 218 represents the TaN_x/Ta structure where the overlying Ta layer was 456 Å thick.

The XRD scanning of these specimens was done using the standard θ - 2θ technique, with the relative normalized area under the Cu {111} intensity peak shown on the scale labeled 203. Curve 202 illustrates the normalized area under the Cu {111} CPS (counts per second) intensity peak for the specimens previously described, with the Ta layer thickness increasing from left to right on the curve beginning with data point 210. A second measurement indicating the amount of the Cu {111} orientation present is provided in the rocking curve data shown on the scale labeled 205. The data represents the Cu {111} FWHM measured in degrees θ.

In the rocking curve measurement technique, the sample is rotating and the detector is rotating. The CPS measurement is made at a set angle and then the detector is slightly rotated and a new CPS is measured. A plot of the CPS at increasing angle of measurement is made, generating a distribution curve of the quantity of the specific

crystal orientation measured at increasing angles.

FWHM = full width half max. FWHM is calculated by measuring the width of the curve at a position on the curve which represents one half of the maximum height of the curve. The FWHM is expressed in degrees and represents the number of degrees spanned by the width of the curve at half of its maximum height. A wider curve (a higher number on the scale), spanning a larger number of degrees, indicates that the signal for the crystallographic orientation of interest is not a strong signal and less copper {111} crystallographic orientation is present. A narrow curve (a lower number on the scale), spanning a limited number of degrees, is a strong signal, indicating a larger quantity of the crystallographic orientation is present. Curve 204 illustrates the FWHM for the specimens previously described, with the Ta layer thickness increasing from left to right on the curve beginning with data point 210.

Data point 206 on curve 202 shows the normalized area under the Cu {111} intensity peak for the specimen having a 500 Å thick Ta layer underlying the 1,000 Å thick sputtered copper layer. As is evident from the curve 202, the quantity of Cu {111} crystal orientation is relatively high. However, as previously mentioned, a layer of pure Ta does not provide a diffusion barrier which performs as well as the TaN_x/Ta barrier layer structure in preventing copper diffusion into the underlying silicon dioxide dielectric layer.

Data point 208 on curve 202 shows the normalized area under the Cu {111} intensity peak for the specimen having a 500 Å thick TaN layer underlying the 1,000 Å thick sputtered copper layer. Although the TaN layer provides a good diffusion barrier, the quantity of Cu {111} is minimal. Data points 210 through 216 on curve 202 show the normalized area under the Cu {111} intensity peak for specimens having a 500 Å thick TaN layer, with increasing thicknesses of an overlying Ta layer (as the data point

number increases), all with a 1,000 Å layer of copper applied over the TaN/Ta barrier layer. The 500 Å TaN/57 Å Ta barrier layer of data point 210 provides about 10% less area under the Cu {111} peak than the 500 Å layer of Ta provided. The exact significance of this decrease in electromigration performance has not yet been determined; however, the difference is not expected to have a significant influence on device performance.

At data point 214 on curve 202, which represents the 500 Å TaN/170 Å Ta barrier layer, the area under the Cu {111} peak is equivalent to the pure layer of Ta. Surprisingly, at some point between the 500 Å TaN/227 Å Ta barrier layer represented by data point 216 and the 500 Å TaN/456 Å Ta barrier layer represented by data point 218, the Cu {111} crystal content increases drastically, rising to a value about 20% greater than that for the pure layer of Ta. The FWHM data shown on curve 204 for the same specimens described above confirms the same trends illustrated by the normalized area under the Cu {111} intensity peak. See, for example, a lower FWHM after data point 216 on curve 204, indicating an increased amount of the copper {111} crystallographic orientation.

Based on this disclosure, one skilled in the art can provide a barrier layer which prevents the diffusion of a copper layer deposited thereover, and enable the formation of a copper layer having a high {111} crystallographic content.

The above described preferred embodiments are not intended to limit the scope of the present invention, as one skilled in the art can, in view of the present disclosure expand such embodiments to correspond with the subject matter of the invention claimed below.

CLAIMS

We claim:

1. A barrier layer for use in combination with a conductive layer, said barrier layer having a particular structure comprising:

a) a first layer of TaN_x having a thickness ranging from greater than about 10 Å to about 1,000 Å; and

b) a second layer of Ta overlying said first layer and having a thickness ranging from about 5 Å to about 500 Å.

2. The barrier layer of Claim 1, wherein the conductive layer is copper.

3. The barrier layer of Claim 1, wherein said barrier layer is used in an interconnect structure, and wherein the thickness of said TaN_x layer ranges from about 50 Å to about 1,000 Å and the thickness of said Ta layer ranges from about 20 Å to about 500 Å.

4. The barrier layer of Claim 1, wherein said barrier layer is used in a contact via structure, and wherein the thickness of said TaN_x layer ranges from about 10 Å to about 300 Å and the thickness of said Ta layer ranges from about 5 Å to about 300 Å.

5. The barrier layer of Claim 2, or Claim 3, or Claim 4, wherein x ranges from about 0.1 to about 1.5.

6. A copper interconnect structure comprising the barrier layer of Claim 2 and an overlying copper layer, wherein the Cu {111} crystallographic content of said overlying copper layer is at least 70% of the Cu {111} crystallographic content which can be obtained using a pure Ta barrier layer which is about 500 Å thick.

7. A copper contact via-comprising structure including the barrier layer of Claim 2 and a copper fill, wherein the copper fill layer Cu {111} crystallographic content is at least 70% of the Cu {111} crystallographic content which can be obtained using a pure Ta barrier layer which is about 250 Å thick.

8. A method of producing a barrier layer useful in combination with a conductive layer, said method comprising the steps of:

a) depositing a first layer of TaN_x having a thickness ranging from greater than about 10 Å to about 1,000 Å; and

b) depositing a second layer of Ta having a thickness ranging from about 5 Å to about 500 Å.

9. The method of Claim 8, wherein the conductive layer is copper.

10. The method of Claim 8, wherein said first layer of TaN_x is deposited upon a substrate having a substrate temperature ranging from about 25°C to about 500°C.

11. The method of Claim 8, wherein said second layer of Ta is deposited upon a substrate having a substrate temperature ranging from about 25°C to about 500°C.

12. The method of Claim 8, wherein said barrier layer is used in an interconnect structure, and wherein the thickness of said TaN_x layer ranges from about 50 Å to about 1,000 Å and the thickness of said Ta layer ranges from about 20 Å to about 500 Å.

13. The method of Claim 8, wherein said barrier layer is used in a contact via structure, and wherein the thickness of said TaN_x layer ranges from about 10 Å to about 300 Å and the thickness of said Ta layer ranges from about 5 Å to about 300 Å.

14. The method of Claim 8, or Claim 12, or Claim 13, where x ranges from about 0.1 to about 1.5.

15. The method of Claim 8, wherein at least a portion of said Ta layer is deposited using a traditional, standard sputtering technique.

16. The method of Claim 12, wherein at least a portion of said Ta layer is deposited using a traditional, standard sputtering technique.

17. The method of Claim 8, wherein at least a portion of the TaN_x layer is deposited using a traditional, standard sputtering technique.

18. The method of Claim 8, wherein at least a portion of said Ta layer is deposited using ion-deposition sputtering.

19. The method of Claim 13, wherein at least a portion of said Ta layer is deposited using ion-deposition sputtering.

20. The method of Claim 8, wherein at least a portion of the TaN_x layer is deposited using ion-deposition sputteirng.

21. A method of producing a copper interconnect structure comprising the barrier layer of Claim 1 and an overlying copper layer, wherein the Cu {111} crystallographic content of said overlying copper layer is at least 70 % of the Cu {111} crystallographic content which can be obtained by depositing said copper layer using a pure Ta barrier layer which is about 500 Å thick, said method comprising the steps of:

a) depositing a first layer of TaN_x having a thickness ranging from greater than about 50 Å to about 1,000 Å;

b) depositing a second layer of Ta having a thickness ranging from about 5 Å to about 500 Å over the surface of said first layer of TaN_x; and

c) depositing a third layer of copper over the surface of said second layer of Ta, wherein at least a portion of said third layer of copper is deposited using a physical vapor deposition technique, and wherein the substrate temperature at which said third layer of copper is deposited is less than about 500°C.

22. The method of Claim 21, wherein said copper interconnect structure is annealed at a temperature of less than about 500°C.

23. A method of producing a copper-comprising contact via structure comprising the barrier layer of Claim 1 and an overlying copper layer, wherein the Cu {111} crystallographic content of said overlying copper layer is at least 70% of the Cu {111} crystallographic content which can be obtained by depositing said copper layer using a pure Ta barrier layer which is about 300 Å thick, said method comprising the steps of:

a) depositing a first layer of TaN_x having a thickness ranging from greater than about 10 Å to about 300 Å;

b) depositing a second layer of Ta having a thickness ranging from about 5 Å to about 300 Å over the surface of said first layer of TaN_x; and

c) depositing a third layer of copper over the surface of said second layer of Ta, wherein at least a portion of said third layer of copper is deposited using a physical vapor deposition technique, and wherein the substrate temperature at which said third layer of copper is deposited is less than about 500°C.

24. The method of Claim 23, wherein said contact-comprising structure is annealed at a temperature of less than about 500°C.

25. The method of Claim 23, wherein said copper layer is deposited at a temperature of less than about 300°C.

26. The method of Claim 25, wherein said structure is annealed at a temperature of less than about 500°C.

27. A method of producing a copper-comprising contact structure including the barrier layer of Claim 1 and an overlying copper layer, wherein the Cu {111} crystallographic content of said overlying copper layer is at least 70% of the Cu {111} crystallographic content which can be obtained by depositing said copper layer using a pure Ta barrier layer which is about 300 Å thick, said method comprising the steps of:

a) depositing a first layer of TaN_x having a thickness ranging from greater than about 10 Å to about 300 Å;

b) depositing a second layer of Ta having a thickness ranging from about 5 Å to about 300 Å over the surface of said first layer of TaN_x; and

c) depositing a third layer of copper over the surface of said second layer of Ta, wherein at least a portion of said third layer of copper is deposited using a physical vapor deposition technique, and wherein the substrate temperature at which said third layer of copper is deposited is less than about 500°C,

wherein at least a portion of said first layer, or said second layer, or said third layer, or a combination thereof, is deposited using ion-deposition sputtering.

ABSTRACT OF THE DISCLOSURE

Disclosed herein is a barrier layer structure useful in forming copper interconnects and electrical contacts of semiconductor devices. The barrier layer structure comprises a first layer of TaN_x which is applied directly over the substrate, followed by a second layer of Ta. The TaN_x/Ta barrier layer structure provides both a barrier to the diffusion of a copper layer deposited thereover, and enables the formation of a copper layer having a high {111} crystallographic content so that the electromigration resistance of the copper is increased. The TaN_x layer, where x ranges from about 0.1 to about 1.5, is sufficiently amorphous to prevent the diffusion of copper into the underlying substrate, which is typically silicon or a dielectric such as silicon dioxide. The thickness of the TaN_x and Ta layers used for an interconnect depend on the feature size and aspect ratio; typically, the TaN_x layer thickness ranges from about 50 Å to about 1,000 Å, while the Ta layer thickness ranges from about 20 Å to about 500 Å. For a contact via, the permissible layer thickness on the via walls must be even more carefully controlled based on feature size and aspect ratio; typically, the TaN_x layer thickness ranges from about 10 Å to about 300 Å, while the Ta layer thickness ranges from about 5 Å to about 300 Å. The copper layer is deposited at the thickness desired to suit the needs of the device. The copper layer may be deposited using any of the preferred techniques known in the art. Preferably, the entire copper layer, or at least a "seed" layer of copper, is deposited using physical vapor deposition techniques such as sputtering or evaporation, as opposed to CVD or electroplating. Since the crystal orientation of the copper is sensitive to deposition temperature, and since the copper may tend to dewet/delaminate from the barrier layer if the temperature is too high, it is important that the copper be deposited and/or annealed at a temperature of less than about 500°C, and preferably at a temperature of less than about 300°C.

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XRD of Cu {111} on TaN_x/Ta Substrate

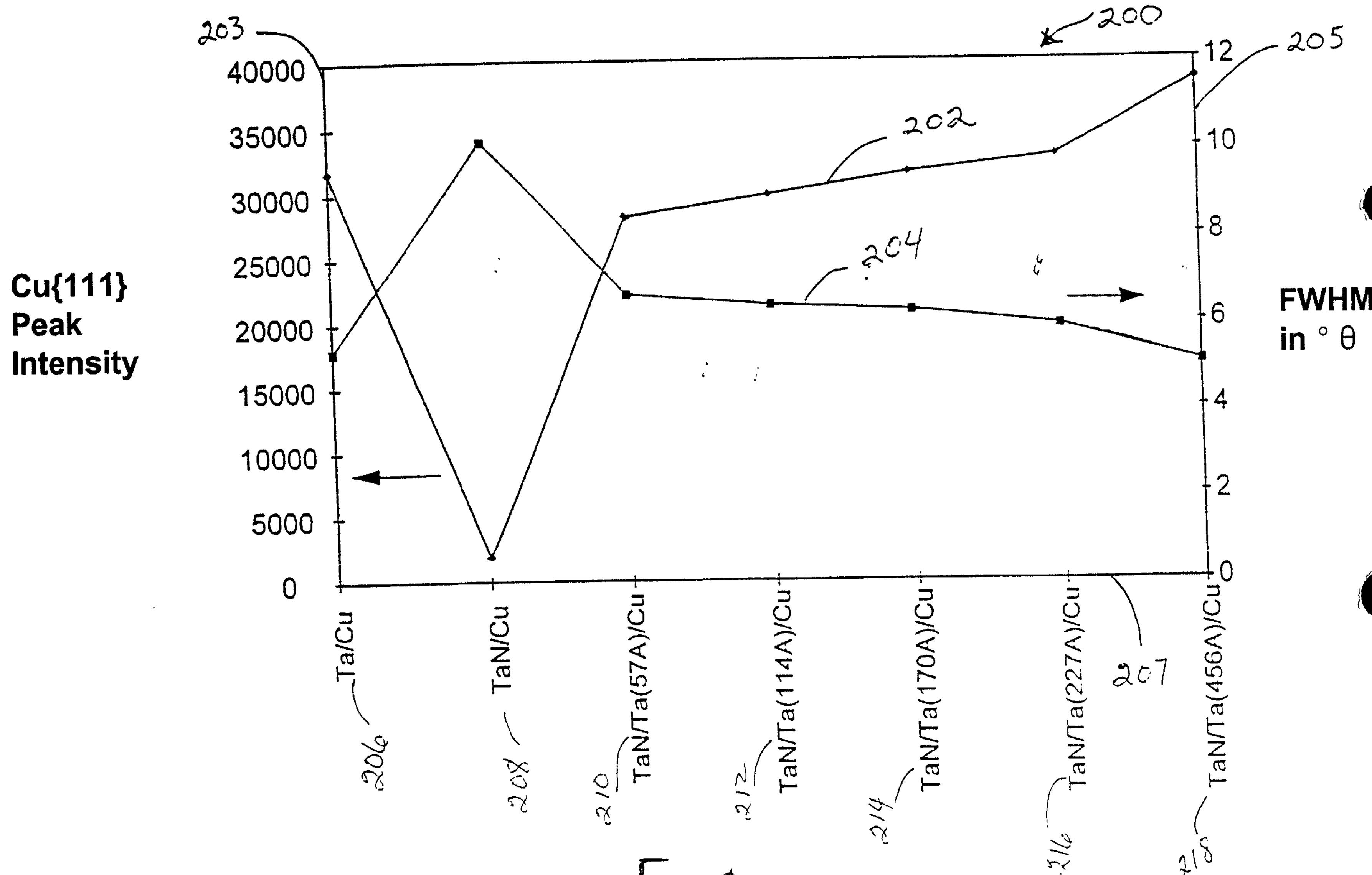

Fig. 2

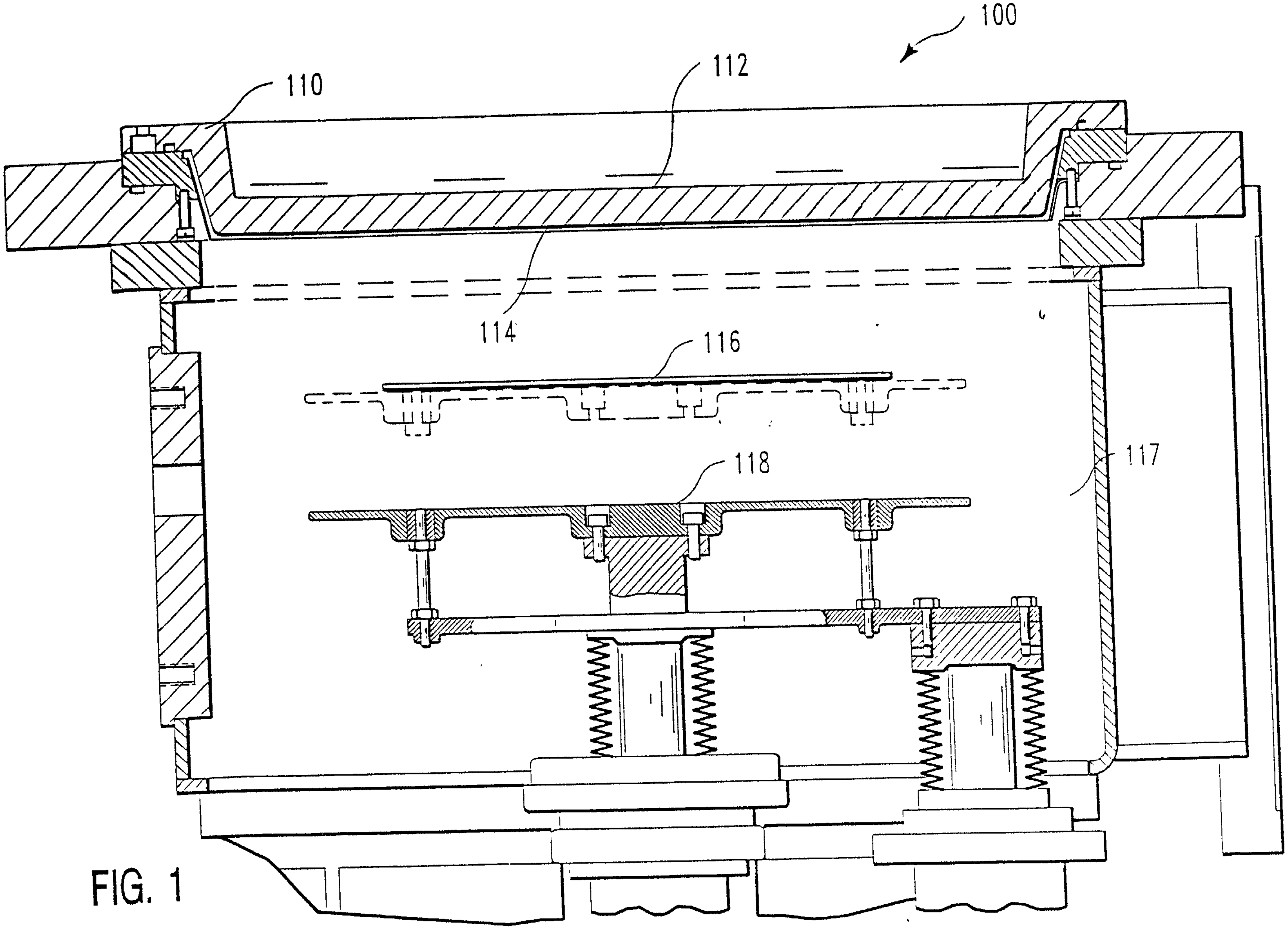

FIG. 1

PATENT APPLICATION

DECLARATION AND POWER OF ATTORNEY
Original Application

As below named inventor, I declare that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in this Declaration, that the information given herein is true, that I believe that I am the original, first and sole inventor of the invention entitled:

A TAILORED BARRIER LAYER WHICH PROVIDES IMPROVED COPPER INTERCONNECT ELECTROMIGRATION RESISTANCE

which is described and claimed in:

X the attached specification or

__ the specification in application Serial No. _______ filed ________________ amended ______

that I acknowledge my duty to disclose information in accordance with 37 C.F.R. Section 1.56 and defined on the attached sheet, which is material to the examination of this application, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, or in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application and that as to applications for patent or inventor's certificate filed by me or my legal representatives or assigns in any country foreign to the United States of America, the earliest filed foreign applications(s) filed within twelve months prior to the filing date of this application and all foreign applications filed more than twelve months prior to the filing date of this application, if any, are identified below.

CHECK APPROPRIATE BOX:

X No earlier-filed foreign applications.

__ Required information as to foreign applications filed prior to filing date of this application is on page 5 attached hereto and made a part hereof.

A:\am1776.dec.wpd May 15, 1996

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Name (204) NAME:	Signature	Date

Section 1.56 Duty to Disclose Information Material to Patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by Sections 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applications to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section , information is material to patentability when it is not cumulative to information already of record of being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the application takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claims is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any considerations given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent or inventor.